Formed on the color filter substrate 110 are common electrodes (not shown) which receive a common voltage, and an R,G,B color filter layer (not shown). Formed on the TFT substrate 120 are a plurality of parallel gate lines Gn, or scanning lines, and a plurality of parallel data lines Dm that receive image signals. The gate lines Gn are laid substantially perpendicular to the data lines Dm in an insulated manner. Also, pixel electrodes are formed at corresponding areas where the data lines Dm intersect the gate lines Gn, and a thin film transistor (TFT) 125, which acts as a switching device, is formed at each of the pixels.

Page 11, lines 19-23, please replace with the following:

However, it is also possible to form the first shift clock signal CLK1 and the second shift clock signal CLK2 on different layers of the first PCB 500. Further, the first shift clock signal CLK1 and the second shift clock signal CLK2 may have opposite phases (by a phase difference of 180°) as described above, or may have a phase difference of 90° to 270°.

In the Claims:

Please amend claims 1-11 and 14-17 as follows.

1. (Twice Amended) A liquid crystal display system, comprising:

a liquid crystal display panel including a plurality of data lines, a plurality of gate lines intersecting the data lines, and a plurality of pixel electrodes arranged in a matrix type and each

having a switch connected to one of the gate lines and one of the data lines;

a gate driver for successively applying a gate voltage to the gate lines to turn on the switches;

a data driver for applying a gray voltage, corresponding to image data signals, to the data lines;

a timing controller for sending both the image data signals and a shift clock signal to the data driver,

a first signal wire through which the shift clock signal is transmitted to said data driver; and

a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90° to 270° is transmitted to a ground.

2. (Twice Amended) The liquid crystal display system of claim 1, wherein the second signal wire is connected to the ground through a predetermined resistance value.

3. (Amended) The liquid crystal display system of claim 2, wherein the first clock signal is generated in the timing controller.

4. (Amended) The liquid crystal display system of claim 2, wherein the first signal wire and the second signal wire are provided on a circuit board.

5. (Amended) The liquid crystal display system of claim 4, wherein the circuit board is a multi-layered printed circuit board and the first signal wire and the second signal wire are formed in parallel on the same layer.

6. (Amended) The liquid crystal display system of claim 4, wherein the circuit board is a multi-layered printed circuit board and the first signal wire and the second signal wire are formed on different layers.

7. (Amended) The liquid crystal display system of claim 1, wherein the first clock signal has a 180° phase difference from the shift clock signal.

8. (Amended) The liquid crystal display system of claim 7, wherein the data driver comprises a plurality of data driver integrated circuits for receiving the image data signals and the shift clock signal from the timing controller and applying the gray voltage corresponding to the image data signals to the data lines of the LCD panel.

9. (Amended) The liquid crystal display system of claim 8, wherein the data driver integrated circuits comprise:

a shift register for shifting and storing the image data signals in synchronization with the shift clock signal after receiving the image data signals from the timing controller;

a D/A converter receiving the image data signals stored in the shift register and converting the image data signals to a corresponding gray voltage; and

an output buffer for temporarily storing the gray voltage output from the D/A converter, and applying the gray voltage to the data lines of the liquid crystal display panel line by line.

10. (Amended) A liquid crystal display system, comprising:

a liquid crystal display panel including a plurality of data lines, a plurality of gate lines intersecting the data lines, and a plurality of pixel electrodes arranged in a matrix type and each having a switch connected to one of the gate lines and one of the data lines;

a gate driver for successively applying a gate voltage to the gate lines to turn on the switches;

a circuit board including:

a timing controller for generating a first image data signal and a second image data signal and generating a first shift clock signal and a second shift clock signal with a phase difference of 90° to 270° that respectively shift the first image data signal and the second image data signal;

a first image data signal wire and a second image data signal wire through which the first image data signal and the second image data signal are respectively transmitted; and

a first shift clock signal wire and a second shift clock signal wire through which the first shift clock signal and the second shift clock signal are respectively transmitted;

a data driver receiving the first image data signal and the second image data signal and the first shift clock signal and the second shift clock signal from the timing controller, and applying a gray voltage corresponding to the first image data signal and the second image data signal to the data lines.

11. (Amended) The liquid crystal display system of claim 10, wherein the first image data signals are odd image data signals, and the second image data signals are even image data signals.